CLAIMS

1. A method for memory management in smart card controllers or similar restricted hardware environment by writing of data into a data space in a persistent memory, said method comprising steps of:

a) splitting the persistent memory into blocks with fixed data length having logical block numbers (LBN);

b) selecting the size of blocks as such that it is equal to - or equivalent to an integer ratio of - the length of a page in EEPROM to the physical size of the pages of the EEPROM memory existing on the card;

c) providing a Block Allocation Table (BAT) in order to calculate the physical place of the block in memory from the logical block number;

2. The method according to claim1, including the step of splitting a whole block into individual segments, whereby each fragment is belonging to a different data object.

3. The method according to claim 2, including the step of identifying a corresponding segment through the block number of the whole block and the number of the individual segment.

4. The method according to claim 2, including defining a block header in the block with a list of entries providing information to localize the segments as well as defining their length.

5. The method according to claim 1, wherein a linkage between blocks by writing the LBN of the following block to the header of the leading block is provided.

6. The method according to 1, wherein a secure write mechanism is accomplished by replacing individual memory blocks by each other.

7. The method according to claim 1. wherein some kinds of blocks are organized in form of a ring list.

8. The method according to claim 1 including the step of defining a bit existing in each block header, whereby this bit corresponds to a bit existing in a commit block.

9. The method according to claim 8, where toggling of a bit in the commit block toggles the validity of the corresponding memory block.

10. A device with a persistent memory and a block structure comprising:

a) a memory managing system using a block-oriented memory structure;

b) blocks with the same length and identifying them by their logical block number (LBN);

c) a block allocation table (BAT) to resolve the logical block number to a physical block number (PBN) and its physical address;

11. A device according to claim 10, further comprising a linkage between blocks by writing the LBN of the following block to the header of the leading one.

12. A device according to claim 10 characterized by blocks with fixed block size, which can contain several independent memory segments, belonging to different logical data units.

13. A device according to claim 10 characterized in that the BAT is held in persistent memory (EEPROM).

14. A device according to claim 10 characterized in that the BAT is held in non-persistent memory (RAM-BAT) and re-initialized on startup.